AMENDMENTS TO THE SPECIFICATION

Please amend paragraph 79 as follows:

[0079] Figs. 2 and 6-9 are referenced together in the following discussion of the 30 add/ 30 store example set forth above and illustrated in Fig. 6. The example is discussed below in order to further illustrate the processing of at least one embodiment of the method 200 illustrated in Fig. 2. The example assumes that the ~~memory~~ machine model (see 22, Fig. 1) reflects a target processor with machine resources as follows. The target processor is assumed, for purposes of illustration, to have four memory ports: M0, M1, M2, and M3. It is further assumed that the target processor includes two integer ports (I0 and I1), two floating-point ports (F0 and F1), and three (3) branch ports (B0, B1, B2). It is assumed that add instructions and other general ALU instructions can be scheduled on any of the four memory ports (M0, M1, M2, M3) as well as on either of the two integer ports (I0, I1). Furthermore, it is assumed that store instructions, a sub-class of ALU instructions, can only be scheduled on ports M2 or M3. Accordingly, six ALU instructions may be scheduled per cycle, but only two of those instructions may be store instructions.